

EDUCATION	<i>Ph.D. Computer Science, Iowa State University, USA</i>	2016–2020
	<i>Thesis: Model Checking Large Design Spaces: Theory, Tools, and Experiments</i>	
	<i>Ph.D. Computer Science, University of Cincinnati, USA</i>	2015–2016 (transfer)
	<i>M.S.E. Embedded Systems, University of Pennsylvania, USA</i>	2013–2015
	<i>B.E. Instrumentation and Control, University of Delhi, India</i>	2009–2013
EXPERIENCE	Research and Development Engineer , <i>Full-time, IBM, Austin, TX</i>	Aug 2020 – present
	<i>Formal Verification Algorithms and Tools</i>	
	<ol style="list-style-type: none">1. Develop algorithms and tools to improve formal verification scalability on complex hardware designs.2. Benchmark and evaluate performance of state-of-the-art verification algorithms and software.3. Improve the orchestration, and automation of formal verification algorithms and tools.	
	Research and Development Engineer , <i>Part-time, IBM, Austin, TX</i>	Sep 2019 – Aug 2020
	<i>Sequential Equivalence Checking and Abstraction</i>	
	<ol style="list-style-type: none">1. Develop techniques for equivalence checking by efficient multi-property abstraction, and2. Design algorithms for parallel orchestration in sequential equivalence checking.	
	Formal Verification Engineer , <i>Internship, Apple, Cupertino, CA</i>	May 2019 – Aug 2019
	<i>Formal Verification of SoC Designs</i>	
	<ol style="list-style-type: none">1. Formally verified critical cryptography hardware designs in Apple SoCs, and2. Performed equivalence checking between Haskell-generated C code and Verilog RTL.	
	Research and Development Engineer , <i>Part-time, IBM, Austin, TX</i>	Aug 2018 – May 2019
	<i>Formal Verification of Multi-Property Testbenches</i>	
	<ol style="list-style-type: none">1. Developed techniques to group and partition properties for formal verification, and2. Improved multiple property verification support in IBM's model checker.	
	Formal Verification Engineer , <i>Internship, Apple, Cupertino, CA</i>	May 2018 – Aug 2018
	<i>Software Verification and Theorem Proving</i>	
	<ol style="list-style-type: none">1. Formally verified C code using Isabelle/HOL theorem prover, and2. Developed a custom SMT tactic for word-level and non-linear integer arithmetic.	
	Researcher , <i>Internship, Fondazione Bruno Kessler, Trento, Italy</i>	May 2015 – Aug 2015
	<i>Formal Verification of NextGen Air Traffic Controller</i>	
	<ol style="list-style-type: none">1. Added extensions to include asymmetric information sharing between aircraft,2. Developed a contract-based design case-study of a sample railroad system, and3. Analyzed extraction of SMV models from LLVM bitcode and control flow graphs.	
	Embedded Systems Programmer , <i>Part-time, University of Pennsylvania</i>	Jan 2014 – Apr 2015
	<i>Wireless and Invasive Brain-Computer Interfaces</i>	
	<ol style="list-style-type: none">1. Designed a wireless brain-sensor interface system to control prosthetics, and2. Researched the use of compressive sensing and learning to minimize data outflow.	
	Hardware Designer , <i>Part-time, Texas Instruments, New Delhi, India</i>	Dec 2011 – Apr 2013
	<i>ARM-based Microcontroller Development Platforms</i>	
	<ol style="list-style-type: none">1. Responsible for complete hardware/software design of ARM-based learning kits,2. Commercially launched two learning kits, Stellaris Guru and Stellaris Shuru, and	

PUBLICATIONS *Peer-Reviewed Conferences*

- C1 Rohit Dureja, Arie Gurfinkel, Alexander Ivrii, and Yakir Vizel. IC3 with Internal Signals. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, New Haven, Connecticut, USA, October 2021. IEEE/ACM (**Best Paper Award**)
- C2 Rohit Dureja, Jason Baumgartner, Robert Kanzelman, Mark Williams, and Kristin Y. Rozier. Accelerating Parallel Verification via Complementary Property Partitioning and Strategy Exploration. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, Haifa, Israel, September 2020. IEEE/ACM
- C3 Rohit Dureja, Jason Baumgartner, Alexander Ivrii, Robert Kanzelman, and Kristin Y. Rozier. Boosting Verification Scalability via Structural Grouping and Semantic Partitioning of Properties. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, San Jose, California, USA, October 2019. IEEE/ACM
- C4 Rohit Dureja, Jianwen Li, Geguang Pu, Moshe Y. Vardi, and Kristin Y. Rozier. Intersection and Rotation of Assumption Literals Boosts Bug-Finding. In *Proceedings of Verified Software: Theories, Tools, and Experiments (VSTTE)*, New York, USA, July 2019. Springer, Cham
- C5 Jianwen Li, Rohit Dureja, Geguang Pu, Kristin Y. Rozier, and Moshe Y. Vardi. SimpleCAR: An Efficient Bug-Finding Tool Based On Approximate Reachability. In *Proceedings of Computer Aided Verification (CAV)*, Oxford, United Kingdom, July 2018. Springer, Cham
- C6 Rohit Dureja and Kristin Y. Rozier. More Scalable LTL Model Checking via Discovering Design-Space Dependencies (D^3). In *Proceedings of Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, Thessaloniki, Greece, April 2018. Springer, Cham
- C7 Rohit Dureja and Kristin Y. Rozier. FuseIC3: An Algorithm for Checking Large Design Spaces. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, Vienna, Austria, October 2017. IEEE/ACM
- C8 Rohit Dureja, Eric W. D. Rozier, and Kristin Y. Rozier. A Case Study in Safety, Security, and Availability of Wireless-Enabled Aircraft Communication Networks. In *Proceedings of AIAA Aviation Technology, Integration, and Operations Conference (AVIATION)*, Denver, Colorado, USA, June 2017. AIAA

Journals

- J9 Rohit Dureja, Pei Zhang, Matthew Cauwels, Philip Jones, Joseph Zambreno, and Kristin Y. Rozier. Model Predictive Runtime Verification for Embedded Platforms with Real-Time Deadlines. *ACM Trans. Embedded Computer Systems*
- J10 Rohit Dureja and Kristin Y. Rozier. Incremental Design-Space Model Checking via Resuable Reachable State Approximations. *Formal Methods in System Design*
- J11 Rohit Dureja and Kristin Yvonne Rozier. Formal framework for safety, security, and availability of aircraft communication networks. *Journal of Aerospace Information Systems*, 17(7):322–335, 2020

Patents

- P12 Rohit Dureja, Jason Baumgartner, Alexander Ivrii, and Robert Kanzelman. *Grouping and Partitioning of Properties for Logic Verification*. U.S. Patent 10,789,403

Workshops and Posters

- M13 Rohit Dureja and Kristin Y. Rozier. Scalable Verification of Designs with Multiple Properties. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, San Jose, California, USA, October 2019 (**Best Student Contribution Award**)
- M14 Rohit Dureja and Kristin Y. Rozier. From One to Many: Checking A Set of Models. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, Vienna, Austria, October 2017
- M15 Rohit Dureja and Kristin Y. Rozier. Comparative Safety Analysis of Wireless Communication Networks in Avionics. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, Mountain View, California, USA, October 2016

Books and Book Chapters

B16 Dhananjay V. Gadre, Rohit Dureja, and Shanjit S. Jajmann. *Getting Started with Stellaris ARM Cortex-M Embedded Processors*. Number 8173718814. Universities Press, 1st edition edition, 2013

Theses

T17 Rohit Dureja. *Model Checking Large Design Spaces: Theory, Tools, and Experiments*. Ph.D. Thesis, Iowa State University, 2020 (**Research Excellence Award**)

AWARDS AND HONORS

- Best Paper Award at Formal Methods in Computer-Aided Design (FMCAD) 2021.
- Research Excellence Award by Iowa State University 2019.
- Best Student Contribution Award at Formal Methods in Computer-Aided Design (FMCAD) 2019.
- National Science Foundation travel grant to Verification Mentoring Workshop (VMW) and Computer Aided Verification (CAV) Conference 2016, 2018.
- Travel grant to Formal Methods in Computer-Aided Design (FMCAD) Conference 2016, 2017, 2019.
- Travel grant and registration waiver to Marktoberdorf Summer School 2016.
- Carnegie Mellon University travel grant to CPS V&V Workshop 2016.
- National Science Foundation travel grant to CPS Week 2016.
- *Best Design* and *Top 10 hack* at HackPrinceton 2013.
- University of Delhi academic scholarship, 2009–2013.

PROFESSIONAL SERVICE

Technical Program Committee:

- Formal Methods in Computer-Aided Design (FMCAD) 2022

Artifact Evaluation Committee:

- Tools and Algorithms for Construction and Analysis of Systems (TACAS) 2018

Conference Review:

- Foundation of Software Engineering (FSE) 2021
- Computer-Aided Verification (CAV) 2021, 2020
- NASA Formal Methods Symposium (NFM) 2021, 2019, 2018, 2016
- Autonomous Agents and Multi-agent Systems (AAMAS) 2021
- International Colloquium on Theoretical Aspects of Computing (ICTAC) 2020
- Automated Software Engineering (ASE) 2020
- Tools and Algorithms for Construction and Analysis of Systems (TACAS) 2020, 2018, 2017
- Quantitative Evaluation of Systems (QEST) 2019
- International Conference on Cyber-Physical Systems (ICCPS) 2019
- Design, Automation, and Test in Europe (DATE) Conference 2019

Journal Review:

- Innovations in Systems and Software Engineering (ISSE)
- Journal of Aerospace Information Systems (JAIS)

Grant Proposal Review:

- Semiconductor Research Corporation (SRC) Computer-Aided Design and Test (CADT)

Conference Organizing

- Verification Mentoring Workshop (VMW) at Federated Logic Conference (FLoC) 2022

TECHNICAL
TALKS

- “Grouping and Partitioning of Properties for Formal Verification”, IBM, Austin, TX, May 7, 2019.
- “Formal Verification of Designs with Multiple Properties”, IBM, Austin, TX, December 19, 2018.
- “Theoretical Foundations of the UAS in the NAS Problem.” *Lightning Talk*, NSF CPS PI Meeting, Washington, DC, November 15, 2018.
- “Design-Space Analysis via SAT-based Model Checking.” *Guest Lecture*, COMS 512 - Formal Methods in Software Engineering, Iowa State University, Ames, IA, February 20–22, 2018.
- “Scalable Design Space Analysis for Future Traffic Management.” CPS Challenges for Unmanned and Autonomous Systems Workshop, Washington, DC, November 14, 2017.
- “Making Undecidable Problems Decidable in Practice.” Software Engineering Seminar, Department of Computer Science, Iowa State University, Ames, IA, October 12, 2017.

SELECTED
COURSE
PROJECTS

- *UAV Security Exploit*. Designed a one-click man-in-the-middle (MITM) attack with ARP poisoning to acquire unauthenticated control of a drone.
- *Modeling and Verification of a Pacemaker*. Modeled a pacemaker using UPPAAL and synthesized code to run on a 32-bit ARM microcontroller.
- *Veterinary Patient Records*. Gathered requirements for a patient record system; culminated in a complete requirements specification document, and a prototype.
- *Network Sniffer*. Designed a powerful network packet sniffer capable of collecting socket-connection information and data, SMTP messages and profile connections.
- *Viral Marketing*. Experimentally evaluated the correlation between social network and spread of influence models to maximize information spread.
- *US Presidential Elections*. Designed a predictor model to predict popular vote and electoral college winner of 2016 US presidential elections.

EXTERNAL
TRAINING

- Marktoberdorf School on Dependable Software Systems Engineering, 2016.
- SRI International Sixth Summer School on Formal Techniques, 2016
- RiSE & LogiCS Spring School on Logic and Verification, 2016

REFERENCES Available upon request.